WHAT IS CLAIMED IS:

1. A semiconductor circuit, comprising:

three or more nodes at least including one input node and one output node;

plural paths connected between said three or more nodes and whose signal propagation directions between the nodes are regulated;

a signal propagation time regulator for regulating a signal propagation time of each of said paths;

an input unit for inputting a predetermined input signal to the input node; and

a detector for detecting a time required for the input signal to propagate through said paths and arrive at the output node.

2. The semiconductor circuit according to claim 1, wherein said node comprises a storage unit for, when there are plural signals inputted to said node via paths connected to said node itself, specifying and storing a path of a signal which arrives first or last out of the signals inputted via the paths connected to said node itself.

3. The semiconductor circuit according to claim 2, wherein when three signals are inputted to said node via three paths, said storage unit of said node comprises three three-input negative logical product circuits to each of which one each of the three signals inputted via the three paths is inputted, and

further inputted to said each of the negative logical product circuits are outputs of the other two negative logical product circuits.

4. The semiconductor circuit according to claim 2, wherein said signal propagation time regulator for at least one path out of said plural paths changes the signal propagation time according to a degree of coincidence or a degree of similarity between two signals to be subjected to matching.

5. The semiconductor circuit according to claim 4, wherein said nodes are arranged in a two-dimensional lattice shape.

6. The semiconductor circuit according to claim 5, wherein by detecting the degree of coincidence or the degree of similarity between the two signals to be subjected to matching according to the detected time required to arrive at the output node and specifying a path stored in said storage unit, said detector detects a shortest path or a longest path corresponding to the degree of coincidence or the degree of similarity to perform dynamic programming matching.

7. The semiconductor circuit according to claim 6, wherein when three signals are inputted to said node via three paths, said storage unit of said node comprises three three-input negative logical product circuits to each of which one each of the three signals inputted via the three paths is inputted, and

further inputted to said each of the negative logical product circuits are outputs of the other two negative logical product circuits.

8. The semiconductor circuit according to claim 1, wherein said signal propagation time regulator for at least one path out of said plural paths changes the signal propagation time according to a degree of coincidence or a degree of similarity between two signals to be subjected to matching.

9. The semiconductor circuit according to claim 1, wherein said nodes are arranged in a two-dimensional lattice shape.

10. The semiconductor circuit according to claim 2, wherein by detecting a degree of coincidence or a degree of similarity between two signals to be subjected to matching according to the detected time required to arrive at the output node and specifying a path stored in said storage, said detector detects a shortest path or a longest path corresponding to the degree of coincidence or the degree of similarity to perform dynamic programming matching.

11. The semiconductor circuit according to claim 6, further comprising a converter for converting element values of the two signals to be subjected to matching to pulses having pulse positions according to the element values.

12. The semiconductor circuit according to claim 6, wherein said signal propagation regulator comprises a delay circuit.

13. The semiconductor circuit according to claim 12, wherein said delay circuit comprises an even number of inverters.

14. The semiconductor circuit according to claim 12, wherein said delay circuit is a variable delay circuit.

15. The semiconductor circuit according to claim 6, wherein the two signals to be subjected to matching are character data.

16. The semiconductor circuit according to claim 6, wherein the two signals to be subjected to matching are voice data.

17. The semiconductor circuit according to claim 6, wherein the two signals to be subjected to matching are image data.